Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A digitally compensated digital to analog converter system comprising:

a digital to analog converter;

a storage device for storing anti-function digital coefficients corresponding to an error function of the digital to analog converter; and

an anti-function processor for applying generated anti-function digital coefficients to the digital input of the digital to analog converter for digitally compensating for the error function of the digital to analog converter, said anti-function digital coefficients providing non-linear error compensation.

2. (Original) The digitally compensated digital to analog converter system of claim 1 further including an anti-function coefficient generator system for generating said anti-function digital coefficients.

3. (Original) The digitally compensated digital to analog converter system of claim 2 in which said anti-function coefficient generator system includes an analog to digital converter with its input connected to the output of said digital to analog converter and

said anti-function generator for delivering in, a calibration mode, selected codes through a switching device to said digital to analog converter and receiving from the analog to digital converter a digital representation of the analog output, from said digital to analog converter.

4. (Original) The digitally compensated digital to analog converter system of claim 2 in which said anti-function coefficient generator system includes an anti-function coefficient generator and a switching device for interconnecting said digital anti-function processor with said digital to analog converter in a correction mode and interconnecting said anti-function coefficient generator with said digital to analog converter in a calibration mode.

5. (Original) The digitally compensated digital to analog converter system of claim 4 in which said anti-function generator system includes a storage device for storing the generated anti-function digital coefficients.

6. (Original) The digitally compensated digital to analog converter system of claim 4 in which said anti-function generator system includes a microprocessor.

7. (Original) The digitally compensated digital to analog converter system of claim 1 in which the anti-function digital coefficients are generated from the error function of the digital to analog converter corresponding to the digital input data.

8. (Original) The digitally compensated digital to analog converter system of claim 7 in

which the error function and a digital basis function are used to calculate the anti-function digital coefficients.

9. (Original) The digitally compensated digital to analog converter system of claim 8 in which the digital basis function is a transfer function having multi section output levels.

10. (Original) The digitally compensated digital to analog converter system of claim 8 in which the basis function is a linear transfer function.

11. (Original) The digitally compensated digital to analog converter system of claim 8 in which the digital basis function is an orthogonal basis function.

12. (Original) The digitally compensated digital to analog converter system of claim 1 or 2 wherein said anti-function coefficients are provided by an analog to digital converter measuring an analog output of said digital to analog converter to generate a digital signal supplied to said anti-function coefficient generator.

13. (Original) The digitally compensated digital to analog converter system of claim 3 in which said anti-function generator comprises an Arithmetic Logic Unit (ALU) and control logic with means to implement multiple digital basis functions to provide said anti-function digital coefficients.

14. (Original) The digitally compensated digital to analog converter system of claim 13

wherein said anti-function generator further comprises an optional storage device having anti-function coefficient memory.

15. (Original) The digitally compensated digital to analog converter system of claim 13 wherein said control logic comprises means for providing control signals to said anti-function coefficient generator and to a strobe signal to said analog to digital converter.

16. (Original) The digitally compensated digital to analog converter system of claim 4 wherein said system comprises means for said calibration mode to be re-run a number of times to reduce errors during said correction mode.

17. (Currently amended) A digitally compensated digital to analog converter system comprising:

a digital to analog converter;

an anti-function coefficient generator system for generating anti-function digital coefficients corresponding to the error function of the digital to analog converter; and

an anti-function processor for applying the anti-function digital coefficients to the digital input to the digital to analog converter for digitally compensating for the error function of the digital to analog converter, said anti-function digital coefficients providing non-linear error compensation.

18. (Original) The digitally compensated digital to analog converter system of claim 17 in which said anti-function coefficient generator system includes an anti-function coefficient

generator and a switching device for interconnecting said digital anti-function processor with said digital to analog converter in a correction mode and interconnecting said anti-function coefficient generator with said digital to analog converter in a calibration mode.

19. (Original) The digitally compensated digital to analog converter system of claim 18 in which said anti-function coefficient generator system includes an analog to digital converter with its input connected to the output of said digital to analog converter and said anti-function generator for delivering in said calibration mode selected codes through said switching device to said digital to analog converter and receiving from the analog to digital converter a digital representation of the analog output, from said digital to analog converter.

20. (Original) The digitally compensated digital to analog converter system of claim 19 in which said anti-function generator system includes a microprocessor.

21. (Currently amended) A digitally compensated analog to digital converter system comprising:

an analog to digital converter;

a storage device for storing anti-function digital coefficients corresponding to an error function of the analog to digital converter; and

an anti-function processor for applying generated anti-function digital coefficients to the digital output of the analog to digital converter for digitally compensating for the error function of the analog to digital converter, said anti-function digital coefficients

providing non-linear error compensation.

22. (Currently amended) A digitally compensated signal converter system comprising:

a signal converter;

a storage device for storing anti-function digital coefficients corresponding to an error function of the signal converter; and

an anti-function processor for applying generated anti-function digital coefficients to a digital signal of the signal converter for digitally compensating for the error function of the signal converter, said anti-function digital coefficients providing non-linear error compensation.

23. (Currently amended) A method of digitally compensating a digital to analog converter comprising:

receiving digital input data for a digital to analog converter;

supplying anti-function digital coefficients derived from the error function of the digital to analog converter corresponding to the digital input data; and

applying the anti-function digital coefficients to said digital input data to precondition said digital input data to compensate for the error function of said digital to analog converter, said anti-function digital coefficients providing non-linear error compensation.

24. (Original) The method of claim 23 in which supplying anti-function digital coefficients includes generating said error function.

25. (Original) The method of claim 23 in which generating said error function includes providing a digital input code to said digital to analog converter, measuring the corresponding output of said digital to analog converter and calculating said error function from said measured output of said digital to analog converter.

26. (Currently amended) The method of claim 23 in which supplying anti-function digital coefficients includes selecting a digital basis function from a plurality of digital basis functions, and calculating from said selected digital basis function and said error function the anti-function digital coefficient corresponding to the provided digital output code.

27. (Original) The method of claim 23 comprising the further step of storing said anti-digital coefficients in a storage device.

28. (Original) The method of claim 23 comprising the further steps of: measuring an analog output of said digital to analog converter; providing an analog to digital converter to generate a digital signal from said analog output; and supplying said digital signal to an anti-function coefficient generator.

29. (Original) A method as claimed in claim 28 comprising the step of providing calibrated control signals to said anti-function coefficient generator and to a strobe signal to said analog to digital converter.

30. (Original) A method as claimed claim 29 comprising the additional step of using said calibrated control signals in a calibration mode in a calibration loop defining a calibration cycle, wherein said calibration cycle is run at least once.

31. (Currently amended) A method of generating anti-function digital coefficients for a digital to analog converter comprising:

selecting a digital basis function from a plurality of digital basis functions;

providing a digital input code to the digital to analog converter;

measuring the output of the digital to analog converter corresponding to that input code;

calculating from the measured output the error function of the digital to analog converter; and

calculating from the error function and the selected digital basis function the anti-function digital coefficients.

32. (Currently amended) A method of digitally compensating an analog to digital converter comprising:

receiving analog to digital converter digital signal data;

supplying anti-function digital coefficients derived from the error function of the analog to digital converter corresponding to the digital signal data; and

applying the anti-function digital coefficients to said digital input data to precondition said digital input data to compensate for the error function of said analog to digital converter, said anti-function digital coefficients providing non-linear error

compensation.

33. (Currently amended) A method of digitally compensating a signal converter comprising:

receiving ~~signal converter~~ digital signal data for a signal converter;

supplying anti-function digital coefficients derived from the error function of the signal converter corresponding to the digital signal data; and

applying the anti-function digital coefficients to said digital signal data to precondition said digital signal data to compensate for the error function of said signal converter, said anti-function digital coefficients providing non-linear error compensation.

34. (Currently amended) A computer program embodied on a computer readable medium, the computer program comprising program instructions for causing a computer to perform the method of any one of claims 23, 31, 32 or 33.

35. (Original) A computer program as claimed in claim 34 embodied on a record medium.

36. (Original) A computer program as claimed in claim 34 embodied on a carrier signal.

37. (Original) A computer program as claimed in claim 34 embodied on a read-only memory.